that touches the side of single-crystal-silicon germanium-carbon base region **320**. Transistor **300** also has a silicide layer **324** that touches the top surface of region **322**, and a metal base contact **326** that touches silicide layer **324**.

[0018] As further shown in FIG. **3**, transistor **300** includes an n+ polysilicon emitter region **330** that touches the top surface of single-crystal-silicon germanium-carbon base region **320**, and an n+ emitter region **332** that lies in single-crystal-silicon germanium-carbon base region **320**. (N+ emitter region **332** results from the out diffusion of dopants from n+ emitter region **330** during fabrication.) Transistor **300** additionally includes an isolation region **340** that isolates base region **322** from emitter region **330**, a silicide layer **342** that touches the top surface of region **330**, and a metal emitter contact **344** that touches silicide layer **342**. Transistor **300** operates in a conventional manner.

[0019] One problem with transistor **300** is that semiconductor structure **308**, which has a very thin collector region (**314**), is incompatible with the CMOS DIAC ESD protection structures **100** and **200**, which utilize p-wells and deep n-wells. As a result, there is a need for a DIAC ESD protection structure that is compatible with SiGe HBTS.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. **1** is a cross-sectional view illustrating a prior-art CMOS DIAC ESD protection structure **100**.

[0021] FIG. **2** is a cross-sectional view illustrating a prior-art CMOS DIAC ESD protection structure **200**.

[0022] FIG. **3** is a cross-sectional view illustrating a prior-art silicon germanium (SiGe) hetrojunction bipolar transistor (HBT) **300**.

[0023] FIG. **4** is a cross-sectional view illustrating an example of a SiGe DIAC ESD protection structure **400** in accordance with the present invention.

[0024] FIG. **5** is a cross-sectional view illustrating an example of a SiGe DIAC ESD protection structure **500** in accordance with the present invention.

[0025] FIG. **6** is a cross-sectional view illustrating an example of a SiGe DIAC ESD protection structure **600** in accordance with the present invention.

[0026] FIGS. **7-21** are a series of cross-sectional views illustrating an example of a method of forming the SiGe DIAC ESD protection structures **400**, **500**, and **600** in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0027] FIG. **4** shows a cross-sectional view that illustrates an example of a SiGe DIAC ESD protection structure **400** in accordance with the present invention. Structure **400** is similar to transistor **300** and, as a result, utilizes the same reference numerals to designate the elements which are common to structure **400** and transistor **300**.

[0028] As shown in FIG. **4**, SiGe DIAC ESD protection structure **400** includes semiconductor structure **308** which has a p− substrate **310**, and an n+ buried layer **312** that touches and lies over p− substrate **310**. In addition, semiconductor structure **308** includes an n-type collector region **314** that touches the top surface of n+ buried layer **312**, and a number of shallow trench isolation regions **318** that extend down from the top surface of semiconductor structure **308**.

[0029] As further shown in FIG. **4**, structure **400** also includes a pair of spaced-apart base/emitter structures **410** and **412** that are formed on the top surface of semiconductor structure **308** to touch n-type collector region **314** and a common shallow trench isolation region **318**C. The base/emitter structures **410** and **412** both have a p-type single-crystal-silicon germanium-carbon base region **320** that touches the top surface of n-type collector region **314**, and a p+ polysilicon germanium-carbon base contact region **322** that touches the side of single-crystal-silicon germanium-carbon base region **320**.

[0030] In addition, a first area **314**F of n-type collector region **314** lies below and touches the p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410**, and a second area **314**S of n-type collector region **314** lies below and touches the p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **412**. The first and second areas, **314**F and **314**S, in turn, are laterally spaced apart by only the common isolation region **318**C. Also, a face **320**F of p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410**, and a face **320**S of p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **412** touch isolation region **318**C, directly oppose each other, and are substantially parallel.

[0031] As further shown in FIG. **4**, the base/emitter structures **410** and **412** also both have a silicide layer **324** that touches the top surface of region **322**, and a metal base contact **326** that touches silicide layer **324**. In addition, the base/emitter structures **410** and **412** both have an n+ polysilicon emitter region **330** that touches the top surface of single-crystal-silicon germanium-carbon base region **320**, and an n+ emitter region **332** that lies in single-crystal-silicon germanium-carbon base region **320**. The base/emitter structures **410** and **412** both additionally have an isolation region **340** that isolates base region **322** from emitter region **330**, a silicide layer **342** that touches the top surface of region **330**, and a metal emitter contact **344** that touches silicide layer **342**.

[0032] Further, the metal base contact **326** and the metal emitter contact **344** of base/emitter structure **410** are connected together, and to a pad **414**. Similarly, the metal base contact **326** and the metal emitter contact **344** of base/emitter structure **412** are connected together, and to a pad **416**.

[0033] During normal operation, when pad **414** is connected to ground and pad **416** is connected to a positive voltage less than the breakdown voltage, the positive voltage is also placed on polysilicon germanium base contact region **322** of base/emitter structure **412**, and thereby on single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **412**.

[0034] The positive voltage on single-crystal-silicon germanium-carbon base region **320** forward biases the junction between p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **412** and the n-type collector region **314**, thereby causing holes to be injected into n-type collector region **314**. The injected holes raise the potential on n-type collector region **314**, thereby reverse biasing the junction between n-type collector region **314** and p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410**. The reverse-biased junction blocks charge carriers from flowing from pad **416** to pad **414**.

[0035] In response to an ESD event, however, the reverse-biased junction between n-type collector region **314** and p-type single-crystal-silicon germanium-carbon base region **320** of base/emitter structure **410** breaks down due to avalanche multiplication. The breakdown of the junction causes